**Product Specifications**

- **Modes:** Asynchronous, Asynchronous Stream and Isochronous Stream
- **Core:** Fully synthesizable Register Transfer Level (RTL) VHDL
- **Test Environment:** Reusable Verilog with abundant scenarios
- **Targeted FPGA:** Xilinx Spartan-6 / Virtex-6
- **Clock Frequency:** 50 MHz

**Options:**

- (May be separately priced)
  - **Adaptations:**
    - 32-bit PCI Host Interface possible
    - Interrupt-driven Host Interface
  - **Add-ons:**
    - Generic 32-bit Host Interface
    - An elaborate test suite containing assorted packets and sizes

**Silicon Cores™\**

Core to the Intelligent System™

**Product Highlights**

- Fully compliant with IEEE 1394a-2000 Standard
- **PHY-Link I/F** conforms to the specifications described in the section 5A of IEEE 1394a-2000 standard
- **Half-duplex** mode of operation
- Programmable bus rates of **100 / 200 / 400 Mbps**
- Supports following Packet types: Asynchronous, Asynchronous Stream, Isochronous Stream and Cycle Start
- Supports, in all, 13 Packet Formats - 10 Asynchronous, 1 Asynchronous Stream, 1 Isochronous and 1 Cycle Start
- Maximum payload sizes of **2 K bytes** (Asynchronous) and **4 K bytes** (Isochronous)
- Cycle Master cable
- **4 Kbytes** of Transmit and Receive FIFO
- Supports both **Differentiated** and **Undifferentiated** modes
- Disabling of PHY-Link I/F through LPS output pin
- Restoring of PHY-Link I/F through LinkOn_digital input pin
- Reception of Isochronous Stream Packets regardless of Isochronous period
- Supports transmission of concatenated packets at assorted modes and speeds
- Selective programming of arbitration enhancements through Acceleration Control Request
Host Interface: The Host Interface allows the SI16FWA20 to be easily connected to most 32-bit Host processors. The Host Interface comprises a 32-bit data bus and an 8-bit Address Bus.

Physical Interface: This module provides services to the Transmitter and Receiver, which include gaining access to the serial bus, sending packets, receiving packets, and sending and receiving Acknowledge Packets to and from the PHY. Physical Interface module encodes the output whenever set to the Differentiated mode of operation.

Transmit and Receive FIFO: SI16FWA20 contains a 4 Kbytes FIFO block, which primarily contains two Transmit sub-FIFOS i.e. ATF (Asynchronous Transmit FIFO) and ITF (Isochronous Transmit FIFO) and one Receive sub-FIFO i.e. GRF (General Receive FIFO). This software configurable FIFO unit allows customization of each sub-FIFO for individual applications.

Tx / Rx Controller: The Tx / Rx controller generates signals for controlling Transmit and Receive operations.

Transmitter: The Transmitter retrieves data from either the ATF or the ITF and creates well-formatted serial bus packets to be transmitted through PHY Interface module.

Control and Status Register: This module contains a set of registers, which store vital information meant to configure and program the device.

Receiver: The Receiver takes the incoming data from the Physical Interface module, checks its integrity and ultimately either stores the same into the Receive memory or discards the said packet and sets the appropriate Data Error Bit in the CSR, in case of a corrupt packet.

Cycle Timer and Monitor: This section comprises a Cycle Time Register, which is designed at par with IEEE 1394a-2000 standard. This Cycle Time Register holds the current time-stamp. The Cycle Monitor observes chip activity and handles scheduling of Isochronous data activity accordingly.

CRC Logic: Generates a 32-bit Cyclic Redundancy Check (CRC) sum value during transmission and checks the same during reception. This CRC is generated for the purpose of error detection of packets, for both header as well as data payload. The CRC polynomial is as shown below:

\[ X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1 \]

Acceleration Controller: After every 125 μs, the device allows selective enabling or disabling of arbitration enhancements. Acceleration arbitration indicates start of Nominal Cycle.

Response Check: This module acts as a watchdog for errors that occur relative to different Request and Response packets in the Asynchronous mode of operation. As for example, it indicates errors such as Response Data Error, Type Error, Conflict Error, Address Error or Mismatch In Data Length of Request and Response packets.

LPS Block: The LPS output pin from the device requests the PHY to either enable or disable the PHY-Link Interface. The output characteristics of LPS, if provided by the Link, depend upon whether the interface mode is Differentiated or Undifferentiated. During Differentiated mode of operation, LPS shall be a pulsed output, whilst the Link is alive, whereas in Undifferentiated mode of operation, LPS remains permanently high, as long as the Link remains alive. In both modes, LPS remains low when Link is either inactive or shut down.

Interrupt Control: Available as an option for making the Host interrupt-driven. An Interrupt gets generated whenever any of the 26 bits in the Interrupt Target Register of the CSR gets set through internal logic. Some of the Interrupt types that the device can handle are: Good Packet Received, Header Error, Channel Invalid, Data Error, Format Error, Cycle Start, Cycle Lost, ATF Full, ITF Full, GRF Full, Subaction Gap and Broadcast Configuration Sent.

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