Factsheet

SPI Protocol®

Silicon Cores™

Core to the Intelligent System™

Function Controller

Silicon Interfaces' SPI protocol specification supports high speed data transfer as per the peripheral specification, making it ideal for high-performance applications that require fast data transfer rates.

- **SPI** is implemented as a microcontroller to communicate with the multiple peripheral devices.
- **SPI** provides capability to transfer the data range up to 64 bits.
- **SPI** can transfer the data at High speed (60MHz) depending on capacity of the peripheral device clock speed.

SPI stands for Serial Peripheral Interface. It is full-duplex communication protocol. It is a synchronous serial communication interface that allows a microcontroller to communicate with peripheral devices, such as sensors, displays, and memory devices.

SPI can transfer the data at High speed is depending on the capacity of the peripheral device clock speed for example SD card clock speed is 25MHz to 50MHz and EEPROM clock speed is 10MHz similarly SPI master will generates the SCLK based on the depending on the peripheral clock speeds.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core.
- Test Bench. (Environment Variable: UVM)
- Targeted FPGA Xilinx Series 7 FPGA
- Clock Frequency: IP core clocks are adjustable (60 MHz for internal)
- Standard IO

Options:

(May be separately priced)

Adaptations:

√ Dual-SPI two data lines are available for data transfer

√ 8/64-Bit Standard Microcontroller Interface possible

Add-ons:

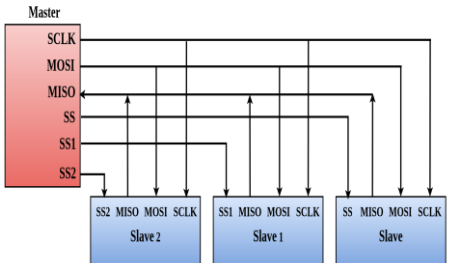
√ Verification IP – UVM VIP

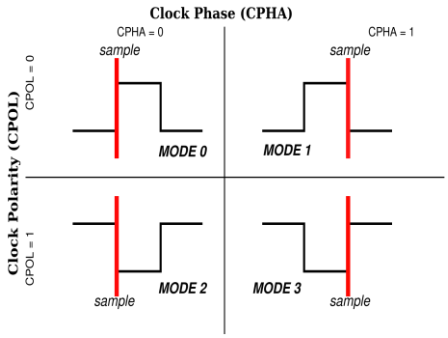
SPI mode is selected based on the CPOL (clock polarity) and CPHA (clock phase) which determines the data latching and data shifting edges whether rising or falling edge and timing and synchronization.

SPI Mode	Clock Polarity	Clock Phase	Data is Latched at	Data is shifted at
0	0	0	Rising Edge	Falling Edge
1	0	1	Falling Edge	Rising Edge
2	1	0	Rising Edge	Falling Edge
3	1	1	Falling Edge	Rising Edge

Product Highlights

- ☑ Full-duplex Serial communication
- ☑ MOSI,MISO are used for the data transfer between master and slave
- ☑ CPOL,CPHA which determines the timing and synchronization
- ☑ SPI is often to use to interface with non-volatile memory devices, such as EEPROM or flash memory.
- ☑ Analog-to-Digital converts and Digital-to-Analog converts can use SPI to transfer data from the microcontroller
- ☑ SPI can capability to transfer data range up to 64 bits.
- ☑ SPI maximum clock frequency is up to 60MHz.





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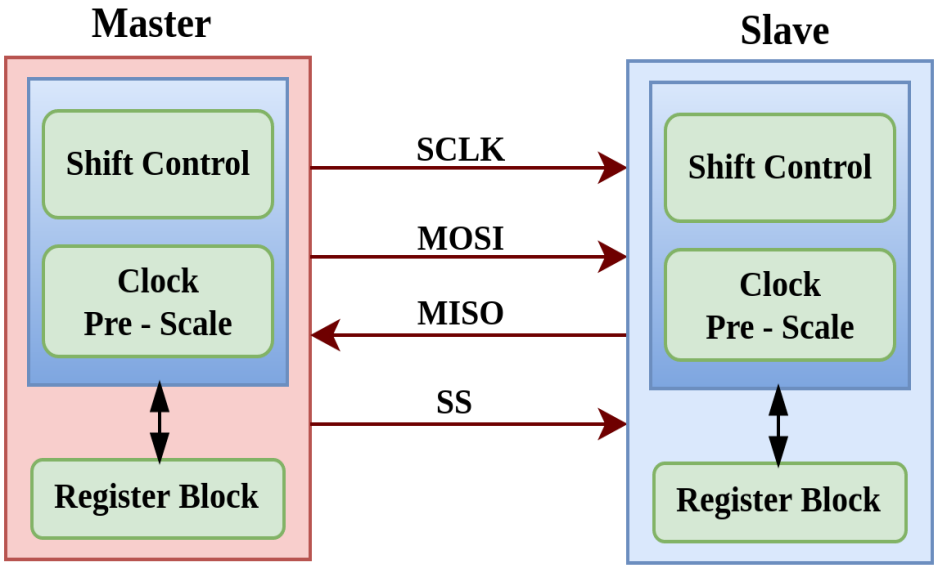
SPI Block Representative



The SPI function core consists of four main modules: SPI interface, SPI master module, SPI slave module, SPI top module.

- SPI Interface: The top-level signals are declared in the interface and the direction of the signals has been defined in the modport for the proper synchronization and to avoid the race-condition between master and slave modules.
- SPI Master: The module includes a struct that defines the master's data and two tasks that handle the SPI communication for two different modes (0/2 and 1/3) of the protocol. The master's data is randomized, and the constraints ensure that the data is valid for the SPI protocol's mode. The master's data is shifted out on the MOSI line while the MISO line receives the slave's data. The data shifting occurs either at the positive edge or negative edge of the SPI clock (SCLK) depending on the SPI mode. The tasks monitor the SS line (slave select) and, when it goes low, start the SPI communication. The tasks continue shifting data until they receive data from the slave, and then they end the communication by raising the SS line.
- SPI Slave: The module includes two tasks for implementing the slave mode 0/2 and mode 1/3 data transfer protocols, respectively. The tasks use the interface to communicate with the master device. The tasks sample the data at the appropriate edge of the SCLK signal and shift the data on the opposite edge. They also use the "SPI_MASTER" module to verify the received data from the master device.
- SPI Top: The module includes the instantiation of the interface, master module and the slave module for the interaction of the master and slave communication.

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