Factsheet

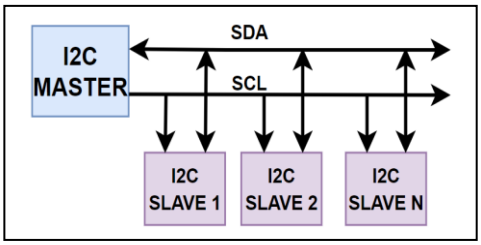
I2C Protocol®

Silicon Cores™

Core to the Intelligent System™

Function Controller

Silicon Interfaces



The I2C (Inter-Integrated Circuit) protocol is a widely used serial communication protocol for transferring data between electronic devices. It was developed by Philips in the 1980s and is now owned by NXP Semiconductors. I2C uses two bidirectional data lines called SDA (Serial Data) and SCL (Serial Clock) for communication between devices. It allows multiple devices to be connected to the same bus, and each device can be identified by a unique address. The protocol supports data transfer rates ranging from a few kilobits per second to several hundred kilobits per second.

I2C is commonly used in embedded systems, especially for connecting sensors, LCD displays, and other peripherals. It is also used in communication between microcontrollers and various ICs such as EEPROMs, ADCs, DACs, and more.

The protocol supports two modes of operation: master and slave. In the master mode, the master device initiates the communication and controls the SCL line. In the slave mode, the slave device responds to the master's requests.

Overall, I2C is a reliable, efficient, and widely adopted communication protocol that facilitates seamless data transfer between different electronic devices.

Product Specifications

- RTL Design (System Verilog).
- Test Bench (Universal Verification Methodology (UVM))
- Clock Frequency: IP core baudrates are adjustable (100kb/ps, 400kb/ps, 1Mb/ps and 3.2Mb/ps)
- Compatible with 8 bit Micro-controller.

Options:

Adaptations:

√ Generic 8-Bit 8051 Microcontroller Interface available

√ PCI/AXI possible

Add-ons:

√ Verification IP – UVM VIP

Product Highlights

- ☑ Protocol is robust in terms of data bytes transfer.
- ☑ Multi slaves' connection possible.
- ☑ Multi-mode baud rates (100kb/ps, 400kb/ps, 1Mb/ps and 3.2Mb/ps) selection available.
- ☑ Include error detection mechanisms such as Acknowledge bits is available to ensure data integrity and reliability.
- ☑ Bi-Directional Communication using the same 2 wire (SDA, SCL) bus.
- ☑ Generic 8-Bit Micro controller Interface.

I2C Protocol Packet Format:

- Start Bit: a single condition that signals the start of a transmission.
- Slave Address: the address of the device being addressed in the transmission, either 7 bits or 10 bits in length depending on the configuration.
- R/W Bit: a single bit that indicates whether the transaction is a read or write operation.
- Address Acknowledge: a single bit that signals whether the receiver has acknowledged the Address.
- Data Byte: one or more bytes of data being transmitted between devices.
- Data Acknowledge: a single bit that signals whether the receiver has acknowledged the Data.
- Stop Bit: a single bit that signals the end of a transmission.

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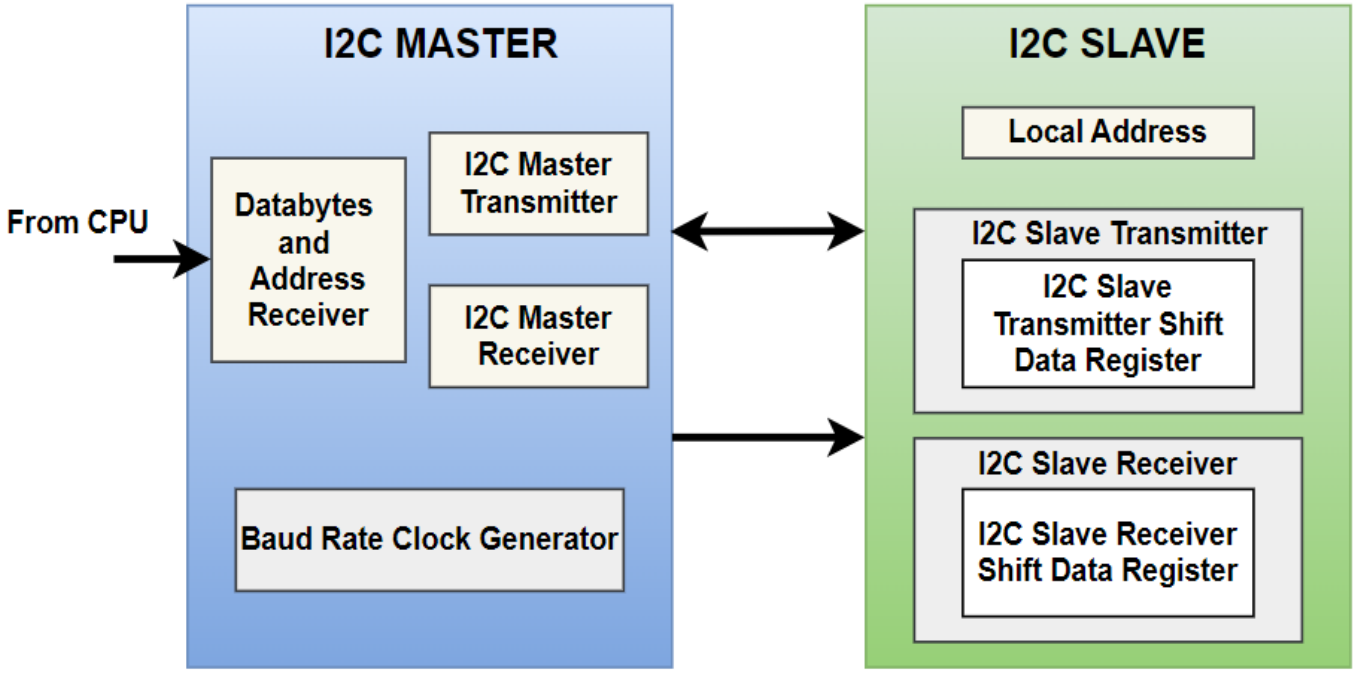
I2C Protocol Block Representative



The I2C Protocol core consists of 2 modules: I2C Master , I2C Slave.

- I2C Master Module: An I2C master controller is a device that functions as the master in an I2C communication system. It generates the clock signal and initiates the data transfer with the slave devices. The master controller typically contains a hardware module that handles the low-level details of the I2C communication, such as generating the start and stop signals, addressing the slave devices, and transmitting and receiving data. In addition to the basic functionality provided by the I2C specification, many I2C master controllers also include additional features to enhance their flexibility and ease of use. For example, some controllers may support multiple speed modes, allowing them to communicate with devices that operate at different clock speeds. Others may include built-in buffer memory to store data being transmitted or received.
- I2C Slave Module: An I2C slave module is a device that acts as a peripheral in an I2C communication system. It receives commands and data from the I2C master controller and responds accordingly. The I2C slave module typically contains a hardware module that handles the low-level details of the I2C communication, such as detecting start and stop signals, detecting its own address, and transmitting and receiving data. The I2C slave module is typically connected to the I2C bus via two pins - SDA (data line) and SCL (clock line). The slave module is addressed by the master controller using a unique 7-bit or 10-bit address, depending on the addressing mode used by the master.

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